IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	09/000,626
Applicant	:	Rajesh RENGARAJAN et al.
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Examiner	:	Tran, Thien F.
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Docket No.	:	97/P/7971/US (0928.0120C)
Customer No.	:	
Title	:	RECESSED SHALLOW TRENCH ISOLATION STRUCTURE NITRIDE LINER AND METHOD OF MAKING SAME

APPELLANT'S BRIEF

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Commissioner for Patents
P.O. Box 1450
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Sir:

This Brief is filed pursuant to the Notice of Appeal filed August 2, 2004.

1. Real Parties In Interest:

The real party in interest is Siemens Aktiengesellschaft, the assignee of the entire title and interest in and to the subject application by virtue of an assignment recorded at the U.S. Patent and Trademark Office at Reel 9503, Frame 0586.

2. Related Appeals and Interferences:

There are no related Appeals or Interferences.

3. Status of Claims:

Claims 1-5, 7, 24 and 25 are on appeal and stand rejected under 35 U.S.C. §103(a). Claims 6 and 8-23 have been canceled. A complete copy of the current claims appears in the attached Appendix.

4. Status of Amendments:

An Amendment was filed on August 2, 2004 with the Notice of Appeal and after the Final Office Action mailed April 1, 2004 (hereinafter, "Final Office Action"). The Amendment was entered, as indicated by the Examiner's Advisory Action mailed August 30, 2004. Claims 12-23 were canceled in the Amendment.

The Amendment further corrected the typographical errors to claims 4 and 5 as presented in the previous Amendment filed October 27, 2003, which resulted in an objection by the Examiner in the Final Office Action due to an inconsistency with the original recited language of these claims. In particular, claim 4, as presented in the Amendment filed October 27, 2003, incorrectly recited the term "nitride layer" (at line 3, should be --nitride liner--) and claim 5 incorrectly recited "said liner, substantially on a top" (lines 2-3, should be --said nitride liner, substantially to a top--). The inconsistency of claims 4 and 5, as presented in the Amendment filed October 27, 2003, has been corrected in the Amendment filed August 2, 2004. These claims have been corrected in accordance with the Examiner's requirements and should thus overcome the objection raised in the Final Office Action. Further, since claims 4 and 5 have been corrected for consistency purposes and not amended, the "Original" claim designation was maintained for these claims in the Amendment filed August 2, 2004.

The remaining claims (i.e., claims 1-3, 7, 24 and 25) were not changed relative to their immediate prior version.

5. Summary of the Invention:

The claims on appeal are directed to shallow trench isolation structures utilized in semiconductor memory devices. In particular, the claims on appeal are directed to shallow trench isolation structures that prevent hot carrier effects due to charge trapping.

As noted in the "Background of the Invention" section of the Specification (pages 1-3), transistors are typically implemented in wells of substrates of an integrated circuit dye. In certain types of circuits, the wells are separated by shallow trench isolation structures, such as the structure shown in Figs. 1, 2, 3A and 3B. A shallow trench isolation structure 100 is

typically formed by depositing pad oxide and nitride layers 106 and 108 onto the substrate, forming a photoresist layer above the pad nitride layer 108, and forming a trench 104 within the substrate by an etching process. An active oxide layer 112 and nitride liner 114 are then formed along the surfaces of the trench 104, with the nitride liner 114 extending over a portion of the pad nitride layer 108 (see Fig. 1). An oxide fill 202 is then formed within the trench 104 and planarized to be substantially planar with the nitride liner 114 (see Fig. 2), followed by stripping away the pad nitride layer 108 and the portion of the nitride liner 114 disposed over the pad nitride layer (see Fig. 3A). A gate oxide 304 and gate polysilicon 306 are then deposited over the pad oxide layer 106 to form a transistor gate (see Fig. 3B).

During stripping of the nitride layer 108 and a portion of the nitride liner 114, some over-etching of the nitride liner 114 can occur, resulting in the nitride liner 114 being recessed within the trench 104 and the formation of a divot region 302 defined between the oxide fill 202 and the vertical walls of the trench 104 (see Figs. 3A and 3B). This in turn results in a portion of the gate oxide 304 and gate polysilicon 306 being deposited within the divot region 302. As noted in the specification (see page 2, line 25 to page 3, line 2), it is difficult to control the depth of the divot region 302, and thus the amount of polysilicon that wraps around the gate. This in turn adversely affects the performance of the transistors formed adjacent the shallow trench isolation structure.

As further noted in the specification (see page 3, lines 3-26), hot carrier reliability problems can occur when P-FET channels are located near the shallow trench isolation structure and the nitride liner is disposed within a depth of the trench as measured from the top of the substrate that overlaps with the P-FET channel depth Dc (see Fig. 3A). In particular, when the nitride liner overlaps with the adjacent P-FET channel depth Dc, the nitride liner can trap or collect charges that should otherwise traverse P-FET channels located near the shallow trench isolation structure. Thus, it is important to ensure that the distance or depth from the substrate surface to the nitride liner within the trench is greater than a channel depth Dc of a transistor disposed in a well adjacent the shallow trench isolation structure.

According to the present invention, the problem of nitride liner depth is overcome by forming a shallow trench isolation structure where the nitride liner within the trench is recessed

to a depth that is below the transistor channel depth Dc. An exemplary embodiment of forming such a shallow trench isolation structure is described at pages 7-10 of the specification and depicted in Figs. 4-8. As can be seen in Figs. 6-8, a shallow trench isolation structure 200 is formed in accordance with the invention including a nitride liner 704 recessed within a trench 104. The nitride liner 704 is recessed within the trench 104 at a depth (as depicted by dashed line 602 in Fig. 6) that is below the depth Dc of the transistor channel disposed in a well adjacent the trench 104.

6. The Issues On Appeal:

The issue presented on Appeal is:

A. Whether claims 1-5, 7, 24 and 25 are properly rejected under 35 U.S.C. §103(a) as being unpatentable over Japanese Patent No. 57-159038 to Fukuda (hereinafter, "Fukuda") in view of U.S. Patent No. 5,872,045 to Lou et al. (hereinafter, "Lou"), Wolf, *In Silicon Processing for the VLSI Era*, Vol. II, pp. 153 and 154 (hereinafter, "Wolf"), and U.S. Patent No. 5,972,778 to Hamada (hereinafter, "Hamada").

7. Grouping Of Claims:

Claims 1 and 24 may be considered together. Claims 2-5 and 7 stand or fall with claim 1. Claim 25 stands or falls with claim 24.

8. Argument:

(i) Rejections Under 35 U.S.C. §103(a)

35 U.S.C. §103(a) states (in pertinent part):

"(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject

> matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains..."

The Supreme Court in Graham v. John Deere, 148 U.S.P.Q. 459 (1966), stated that the obviousness or non-obviousness of subject matter is determined in view of the scope and content of the prior art, the differences between the prior art and the claims at issue and the level of ordinary skill in the pertinent art. Secondary considerations, such as commercial success, long felt but unsolved needs, failure of others, etc., might be utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented. See M.P.E.P. §2141.

The following tenets of patent law must be adhered to when applying 35 U.S.C. §103:

(A) The claimed invention must be considered as a whole;

(B) The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination;

(C) The references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and

(D) Reasonable expectation of success is the standard with which obviousness is determined. Hodosh v. Block Drug Co., Inc., 229 U.S.P.Q. 182, 187 n.5 (Fed. Cir. 1986); See M.P.E.P. §2141.

The basic criteria to establish a *prima facie* case of obviousness, include: some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings; a reasonable expectation of success; and the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. In re Vaeck, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); See M.P.E.P. §2142. Three possible sources for a motivation to combine references include the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art. In re Rouffet, 47 U.S.P.Q.2d 1453, 1457-58 (Fed. Cir. 1998); See M.P.E.P. §2143.01.

A. Claims 1-5, 7, 24 and 25 are improperly rejected under 35 U.S.C. §103(a) as being unpatentable over Fukuda in view of Lou, Wolf, and Hamada.

Independent claim 1 recites a shallow trench isolation structure in a substrate, where the shallow trench isolation structure comprises: a trench in the substrate, and a nitride liner recessed within the trench, the nitride liner forming a partially enclosed volume, and the partially enclosed volume being completely filled with a dielectric material which completely fills the trench. Claim 1 further recites that the nitride liner is recessed such that an uppermost surface of the nitride liner is recessed to a first depth that is greater than a transistor channel depth, Dc, of a transistor that is disposed in a well beside the shallow trench isolation structure, the recessed nitride liner being dimensioned and configured to prevent hot carrier effects due to charge trapping for charge which traverses a channel of the transistor. In addition, claim 1 recites that the dielectric material includes an oxide disposed above the nitride liner such that the oxide extends above the uppermost surface of the nitride liner to substantially a top surface of the substrate, such that substantially no polysilicon material is disposed within the trench.

Similarly, independent claim 24 recites a shallow trench isolation structure for preventing hot carrier effects due to charge trapping, where the shallow trench isolation structure comprises: a trench in the substrate, an oxide liner formed lining the trench and a top surface of the substrate, and a nitride liner recessed within the trench, the nitride liner forming a partially enclosed volume, and the partially enclosed volume being completely filled with a dielectric material which also completely fills the trench. Claim 24 further recites that the nitride liner is recessed such that an uppermost surface of the nitride liner is recessed to a first depth that is greater than a transistor channel depth, Dc, of a transistor that is disposed in a well beside the shallow trench isolation structure, the recessed nitride liner being dimensioned and configured to prevent hot carrier effects due to charge trapping for charge which traverses a channel of the transistor. In addition, claim 24 recites an oxide fill disposed above the nitride liner, such that the oxide fill extends above and below the uppermost surface of the nitride liner substantially to a top surface of the substrate and completely filling below the uppermost surface, respectively, and that the oxide fill is disposed above the nitride liner such that polysilicon material used in other processing is prevented from entering the trench.

There is no combination of Fukuda, Lou, Wolf and/or Hamada that renders obvious the combined features of each of claims 1 and 24, with particular regard to the recited feature of the nitride liner being recessed such that an uppermost surface of the nitride liner is recessed to a first depth that is greater than a transistor channel depth, Dc, of a transistor that is disposed in a well beside the shallow trench isolation structure.

Fukuda teaches the formation of a V-shaped separation area in a silicon substrate 10, where a nitride film 12' is formed within a V-shaped trench defined in the substrate (see Figs. 4(d) and 4(e) of Fukuda). However, there is no disclosure or suggestion whatsoever in Fukuda of a particular depth to which the uppermost surface of nitride film 12' is recessed within the V-shaped groove. The failure of Fukuda to explicitly disclose such a feature is clearly acknowledged by the Examiner (see page 3, lines 11-13 of the Final Office Action).

None of the additional references relied upon by the Examiner makes up for the deficiencies of Fukuda. Regarding Lou, the Examiner relied upon this reference in the Final Office Action for the teaching of a trench isolation structure formed with an oxide or polysilicon filling the trench. However, there is no disclosure or suggestion in Lou of any nitride liner recessed within a trench as recited in claims 1 and 24, let alone the recited feature of the uppermost surface of the nitride liner being recessed to a first depth that is greater than a transistor channel depth, Dc, of a transistor that is disposed in a well beside the trench. At best, Lou describes a nitride layer 20 that extends the entire depth of (and thus is not recessed within) a trench (see Figs. 8A, 8B, 9 and 10 of Lou).

The Examiner relied upon Wolf and Hamada in the Final Office Action in making the assertion that it would have been obvious to recess the uppermost surface of the nitride film within the V-shaped trench of Fukuda below a transistor channel depth Dc as recited in claims 1 and 24. There is simply no teaching in either Wolf or Hamada that would suggest such a modification to Fukuda as asserted by the Examiner.

Wolf and Hamada were relied upon by the Examiner in the Final Office Action for their combined teachings of known depths of trench isolation structures and channel regions within a semiconductor substrate. In particular, the Examiner relied upon Wolf for its teaching of a shallow trench isolation structure formed in a substrate at a depth of about 5000-8000 angstroms.

The Examiner further relied upon Hamada for its teaching of a channel depth for a semiconductor device ranging from 200 angstroms to 1500 angstroms. Neither Wolf nor Hamada teaches a nitride liner recessed within a trench as recited in claims 1 and 24, let alone the recited feature of the uppermost surface of the nitride liner being recessed to a first depth that is greater than a transistor channel depth, Dc, of a transistor that is disposed in a well beside the trench. However, based upon these teachings, the Examiner asserted the following:

> "With the channel region always formed very shallow near a top surface of a substrate as suggested by Hamada, the trench isolation region formed with a depth at least 5 times deeper than that of the channel region as suggested by Wolf and the nitride liner formed at the bottom of the trench as taught by Fukuda, it is obvious that the modified Fukuda's device provides a nitride liner having its first depth greater than the transistor channel depth."
> *(Final Office Action, page 4, lines 1-6)*

There is simply no reasonable basis for making the above conclusion, absent improper hindsight and reliance upon the disclosure in the subject application, that the teachings of Wolf and Hamada provide motivation for modifying the Fukuda device so as to form a nitride layer within the V-shaped trench at a depth that is greater than a transistor channel depth disposed adjacent the V-shaped trench. Even assuming that trench isolation structures are known to be deeper than transistor channel depths disposed adjacent such structures based upon the combined teachings of Wolf and Hamada, at best this might suggest to one having ordinary skill in the art that the V-shaped trench of Fukuda should be deeper than a channel region disposed adjacent the V-shaped trench. However, this does not immediately suggest to one having ordinary skill in the art that the nitride film formed in the V-shaped trench of Fukuda should necessarily have an uppermost surface that is recessed within the trench below a transistor channel depth Dc as recited in claims 1 and 24. There is simply no teaching, support or motivation whatsoever in any of Wolf, Hamada, or even Lou for that matter, to suggest a modification of the Fukuda device in order to include such a feature.

Thus, the Examiner has not met the *prima facie* burden of obviousness in rejecting claims 1 and 24, since there is no teaching or suggestion in any of the cited references of the recited

recess feature for the nitride liner. The Examiner is clearly using impermissible hindsight vision in view of the claimed invention to reject the claims, and has not provided any reasonable teaching or motivation from any of the cited references that would suggest providing the recess depth feature as recited in claims 1 and 24 for the nitride film disposed within the V-shaped trench of Fukuda.

For all of the foregoing reasons, Appellant respectfully submits that claims 1 and 24 would not have been obvious over Fukuda in view of Lou, Wolf and Hamada. Since claims 2-5, 7 and 25 depend from one of claims 1 and 24 and therefore include all the limitations of their parent claim. Accordingly, these claims would not have been obvious over Fukuda in view of Lou, Wolf and Hamada, based at least upon the previous remarks not above for claims 1 and 24.

9. Conclusion

In view of the foregoing it is submitted that the rejections of claims 1-5, 7, 24 and 25 are improper and should be reversed.

Respectfully submitted,

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APPENDIX

CLAIMS ON APPEAL

1. A shallow trench isolation structure in a substrate, said shallow trench isolation structure comprising:

a trench in said substrate;

a nitride liner recessed within said trench and the nitride liner forming a partially enclosed volume, said partially enclosed volume being completely filled with a dielectric material which also completely fills the trench;

wherein said nitride liner is recessed such that an uppermost surface of said nitride liner is recessed to a first depth that is greater than a transistor channel depth, Dc, of a transistor that is disposed in a well beside said shallow trench isolation structure, the recessed nitride liner being dimensioned and configured to prevent hot carrier effects due to charge trapping for charge which traverses a channel of the transistor;

the dielectric material including an oxide disposed above said nitride liner such that said oxide extends above the uppermost surface of said nitride liner to substantially a top surface of said substrate, such that substantially no polysilicon material is disposed within the trench.

2. A shallow trench isolation structure as recited in claim 1, wherein said transistor is a P-FET transistor.

3. A shallow trench isolation structure in a substrate as recited in claim 1, wherein the uppermost surface of said nitride liner is recessed to a first depth that is greater than about 1000 angstroms below a top surface of said substrate.

4. A shallow trench isolation structure in a substrate as recited in claim 1, further comprising:

an oxide layer disposed within the trench, said oxide layer underlying said nitride liner; and

an oxide fill disposed above said nitride liner such that the nitride liner is encapsulated by the oxide fill and oxide layer.

5. A shallow trench isolation structure in a substrate as recited in claim 4, wherein the oxide fill extends above said uppermost surface of said nitride liner, substantially to a top surface of said substrate, such that substantially no void exists above said uppermost surface of said nitride liner.

6. (Canceled)

7. A shallow trench isolation structure in a substrate as recited in claim 4, wherein the oxide fill includes tetraethylorthosilicate.

8-23. (Canceled)

24. A shallow trench isolation structure for preventing hot carrier effects due to charge trapping, said shallow trench isolation structure comprising:

a trench in the substrate;

an oxide liner formed lining the trench and a top surface of the substrate;

a nitride liner recessed within said trench and the nitride liner forming a partially enclosed volume, said partially enclosed volume being completely filled with a dielectric material which also completely fills the trench;

wherein said nitride liner is recessed such that an uppermost surface of said nitride liner is recessed to a first depth that is greater than a transistor channel depth, Dc, of a transistor that is disposed in a well beside said shallow trench isolation structure, the recessed nitride liner being dimensioned and configured to prevent hot carrier effects due to charge trapping for charge which traverses a channel of the transistor;

an oxide fill disposed above said nitride liner, such that said oxide fill extends above and below the uppermost surface of said nitride liner substantially to a top surface of said substrate and completely filling below the uppermost surface, respectively; and

the oxide fill is disposed above said nitride liner such that polysilicon material used in other processing is prevented from entering the trench.

25. The structure of claim 24, wherein the oxide fill includes tetraethyorthosilicate.